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EXAMINER	
BAKER, STEPHEN M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,943	STOLPMAN, VICTOR J.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-19* is/are allowed.

6)☒ Claim(s) *1-10 and 20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over the published article to Cox et al (hereafter "Cox").

Cox discloses an encoder for generating framed (terminated) rate-compatible punctured convolutional codes (*i.e.* "error reduction codes"), the encoder being implemented by a programmable DSP. The terminated punctured convolutional codeword generated by Cox's encoder is "a codeword defining N codeword elements and K information elements coded at a code rate R-K/(N-P), wherein P is a number of punctured elements of the codeword". The processes of generating the mother code and of puncturing the mother code are shown by Cox as being performed in two separate stages (Figure 7), and the puncturing process is shown using a puncturing table that has a separate puncturing pattern for each rate. A region of DSP program memory with instructions for implementing the mother code encoding process shown by Cox apparently provides "a first storage location for storing an error reduction code mother code". A region of DSP memory for storing the puncturing process table patterns shown by Cox for the highest rate rate-compatible puncturing scheme apparently provides "a second storage location for storing a maximum puncturing sequence S_{max}, wherein S_{max} is the puncture sequence for a maximum code rate R_{max},

and further wherein S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1," here considering the "puncture sequence" to be the "0" bits, which are puncture pattern elements whose positions correspond (in the periodic application of the pattern) to positions of codeword bit to be punctured. In other words, the "0" bits (*i.e.* "the puncture sequence") in Cox's puncturing patterns are positioned such that "the puncture sequence for a maximum code rate ... comprises a subset ... that is a puncture sequence for a minimum code rate," entirely because the puncturing is performed rate-compatibly. Accordingly, a subset (two) of Cox's (three) puncturing pattern *a*(1) bits that are "0" are present in puncturing pattern *a*(2), the third "0" in *a*(1), being replaced by a "1" in *a*(2).

Regarding claim 1, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the rate-compatible punctured convolutional coding disclosed by Cox by using a "first storage location for storing an error reduction code mother code" and a "second storage location for storing a maximum puncturing sequence S_{max}, wherein S_{max} is the puncture sequence for a maximum code rate R_{max}, and further wherein S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1" because the process of generating the mother code and of puncturing the mother code are shown by Cox as being performed in two separate stages, and because the rate-compatible punctured convolutional coding disclosed by Cox is implemented by a processor with programmed instructions.

Regarding claim 2, the DSP for implementing the rate-compatible punctured convolutional coding disclosed by Cox implements processing for both transmitting and receiving the punctured convolutional codes.

3. Claims 1-6 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the published article to Kim et al (hereafter "Kim").

Kim discloses an encoder for generating framed (terminated) rate-compatible punctured convolutional codes (which are "error reduction codes"). The terminated punctured codeword so generated is "a codeword defining N codeword elements and K information elements coded at a code rate R-K/(N-P), wherein P is a number of punctured elements of the codeword". The processes of generating the mother code (figure 1) and of subsequently puncturing the mother code (figure 2) are described by Kim as being performed in two separate stages. The puncturing process shown by Kim uses a puncturing table. A region of program memory with instructions for implementing the mother code encoding process shown by Kim would provide "a first storage location for storing an error reduction code mother code". A region of processor memory for storing the puncturing process table shown by Kim for the highest rate rate-compatible puncturing scheme would provide "a second storage location for storing a maximum puncturing sequence S_{max}, wherein S_{max} is the puncture sequence for a maximum code rate R_{max}, and further wherein S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1". Reference is hereby made to the relevant discussion of puncturing tables for rate-compatible codes, in the rejection citing Cox, above.

Regarding claim 1, Official Notice is given that the convenience of implementing logic such as the logic in a channel coder by means of a processor with programmed instructions was well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the rate-compatible punctured convolutional coding disclosed by Kim by using a "first storage location for storing an error reduction code mother code" and a "second storage location for storing a maximum puncturing sequence S_{max}, wherein S_{max} is the puncture sequence for a maximum code rate R_{max}, and further wherein S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1" because the process of generating the mother code and of puncturing the mother code are shown by Kim as being performed in two separate stages, and because the convenience of implementing logic, such as the logic of a channel coder, by means of a processor with programmed instructions was already well known.

Regarding claim 2, the rate-compatible punctured convolutional coding disclosed by Kim is part of a transmitter for transmitting the punctured convolutional codes.

Regarding claim 3, Kim shows (Figure 2) a punctured code with all parity bits punctured (PT_0).

Regarding claims 4-6, Kim shows (Figure 2) five different code rates, with the codes collectively meeting the recited puncturing limitations.

Regarding claim 26, each bit of the separate puncturing patterns that would be used in a typical arrangement based on puncturing tables would presumably be stored

in a "memory element" (*i.e.* storage location) and each different pattern would presumably not share common storage locations with other patterns.

4. Claims 1, 2, 4-10 and 20-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0126551 to Mantha *et al* (hereafter "Mantha").

Mantha discloses an encoder and decoder for generating rate-compatibly punctured LDPCs, implemented by software, and corresponding decoding arrangements. Each punctured LDPC codeword so generated is "a codeword defining N codeword elements and K information elements coded at a code rate R-K/(N-P), wherein P is a number of punctured elements of the codeword". The processes of generating the mother code (figure 1) and of subsequently puncturing the mother code (figure 2) are described by Mantha as being performed in two separate stages. Mantha describes the use of a puncturing table as "typical" [0136] and instead uses an algorithm based on two parameters in order to generate the puncturing patterns. Because the codes are punctured rate-compatibly, the puncturing patterns used by Mantha must be such that "S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1" [0127].

Regarding claim 1, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the rate-compatible punctured LDPC encoding and decoding disclosed by Mantha by using a "first storage location for storing an error reduction code mother code" and a "second storage location for storing a maximum puncturing sequence S_{max}" because the process of generating

the mother code and of puncturing the mother code are shown by Kim as being performed separately, because Kim teaches the use of puncturing tables storing puncturing sequences to be "typical," and because the encoder and decoder are implemented by software. A region of program memory with instructions for implementing the mother code encoding process shown by Mantha would provide "a first storage location for storing an error reduction code mother code" and a region of processor memory for storing the puncturing process table shown by Mantha for the highest rate rate-compatible puncturing scheme would provide "a second storage location for storing a maximum puncturing sequence S_{max}".

Regarding claim 2, the rate-compatible punctured convolutional coding disclosed by Mantha is part of a transmitter for transmitting the punctured convolutional codes.

Regarding claims 4-6, 21, 22, 24 and 25, Mantha shows [0142] six different code rates, with the codes collectively meeting the recited puncturing limitations.

Regarding claims 7 and 9, each bit of the LDPC code is a "variable" having a codeword polynomial coefficient "degree", and so a bit of a stored puncturing pattern corresponding to bit position in the codeword would be stored in a "memory element storing a variable degree".

Regarding claims 8 and 9, each systematic (i.e. non-parity) bit of the LDPC code corresponds to a "variable node".

Regarding claims 20 and 23, Mantha's encoder and decoder of course require a modulator and demodulator and apparently are envisaged for a transceiver with software for encoding and decoding sharing the same program memory.

Regarding claim 26, each bit of the separate puncturing patterns that would be used in a typical arrangement based on puncturing tables would presumably be stored in a "memory element" (*i.e.* storage location) and each different pattern would presumably not share common storage locations with other patterns.

Allowable Subject Matter

5. Claims 11-19 are allowed.

Response to Arguments

6. Applicant's arguments filed 14 October 2005 have been fully considered but they are not persuasive.

Applicant describes the maximum puncture sequence as "represented by a relatively long sequence of memory elements 54, which are depicted as sequential but need not be stored in physically adjacent areas of a volatile memory. A first puncture sequence S_1 is stored at a first memory element 54a, which is the first memory element of the sequence of memory elements that comprise the maximum rate puncture sequence S_{N-K}. In terms of the matrix H of Figure 1A. A second puncture sequence S_2 is stored at a first 54a and second 54b memory elements, which are the first two memory elements of the sequence of memory elements that comprise the maximum rate puncture sequence S_{N-K}" however the rejected claims are of course not necessarily specific to such a storage scheme, as explained in the rejections. Applicant observes that "S_1 is a subset of S_2, which is a subset of S_3, etc., and all are subsets of S_{N-K}. This

relation is written as $S1 \subseteq S2 \subseteq S3 \subseteq \ldots \subseteq S_{N-K}$." The examiner has demonstrated that the same property of subsets applies to the positions of puncture-indicating values (e.g. the positions of Cox's "0"s) in any set of rate-compatible puncturing patterns.

Regarding Kim, applicant writes "only a single rate encoder and decoder is used for variable coding rates, this statement is seen to apply to both the inner and outer encoder separately, so both the transmitter and the receiver each use an inner and separate outer encoder/decoder to achieve the variable rate codes. Were it otherwise, the code would not be concatenated. *The two encoders/decoders are not seen as combinable with ordinary skill* because the outer code is interleaved prior to application of the inner code." The rejection based on Kim argues that a software implementation of Kim's logic is obvious, which applicant's arguments do not address. Kim's two encoders and two decoders are *already combined,* thus applicant's argument is not coherent.

As applicant does not accurately represent the Official Notice actually given in the rejection citing Kim, i.e. simply that *the advantages of using software (instead of hardwired logic) to perform logic operations were already well known*, applicant's requests for references supporting Official Notice not taken are presumed unintentional. The examiner here asserts the factual basis of the Official Notice is *already evident* to any practitioner by the disclosure of Cox.

As should be clear from the present Office actions discussion of Cox's well-known approach of using a puncturing table with separate entries for each rate of a rate-compatible code combined with the understanding that the rejections based on Kim

and Mantha cite the same well-known approach, the characterization that "the Office Action appears to rely on Kim's description of a puncturing table, shared by the transmitter and receiver, as teaching that the puncture table is used to achieve a maximum code rate and a subset of (the puncture table) is used to achieve a minimum code rate" is incorrect. Each puncturing pattern relied on by the rejections, whether referred to as a single table entry or as one table of a plurality of tables, has been shown to meet the claim limitations simply as a result of being one of a set of rate-compatible puncturing patterns.

Further regarding the rejection citing Mantha, the rejections of claims 7-9 are believed to be clearly stated and misunderstood by applicant.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker
Primary Examiner
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smb